form (c) n^+ type semiconductor regions **17, 171**. More specifically, silicon dioxide films about 1 to 2 μm thick are respectively formed on the surface and the undersurface by plasma CVD. Windows 30 μm wide are formed by selective photoetching at intervals of about 100 μm and then phosphorus (P) diffusion using phosphorus hypochlorite is applied to the whole surface of the semiconductor substrate **14** to form a diffusion region about 20 μm deep with a surface impurity concentration of about 1×10^{26} m^{-3} to 1×10^{27} m^{-3}. Subsequently, phosphorus is selectively diffused in the diffusion regions **15, 151** to form n-type semiconductor regions **18, 181** as shown in FIG. **21**(*d*). A specific process for the purpose comprises the steps of forming silicon dioxide films about 1 to 2 μm thick on the upper and lower surfaces by plasma CVD, forming windows 10 μm wide by selectively removing the film, implanting phosphorus (P) ions with a surface impurity concentration of about 1×10^{23} m^{-3} to 1×10^{25} m^{-3} forming semiconductor about 2 to 10 μm deep using heat treatment, cleaning the surface by removing the oxide film using fluoric acid or the like and then forming p^+ type semiconductor regions **16, 161** about 5 μm thick on the cleaned surface using an epitaxial method, as shown in FIG. **21**(*e*). The p^+ type semiconductor layer **16** contains p-type impurities with a concentration of about 1×10^{25} m^{-3} to 1×10^{26} m^{-3}. When it is difficult to form the p^+ type semiconductor layers **16, 161** with high impurity concentration using only an epitaxial method, the process steps may include forming epitaxial growth regions with an impurity concentration of about 1×10^{20} m^{-3} to 1×10^{22} m^{-3} to increase the impurity concentration of the epitaxial regions by diffusing boron using a normal boron nitride film.

Lastly, electrodes **3, 31** about 5 to 15 μm thick are respectively formed on the p^+ type semiconductor regions **16, 161** by electron beam evaporation or resistance heating to complete the constant-voltage diode, as shown in FIG. **21**(*f*). The constant-voltage diode thus obtained has reverse withstand voltage ranging from 6,000 V to 7,000 V.

Although the above description referred to the use of aluminum and boron as p-type impurities in the process of producing the constant-voltage diodes according to the present invention, gallium may also be used. The n-type impurities were phosphorus, but arsenic and antimony may also be used. Use can also be made of semiconductor elements such as bipolar transistors, MOS transistors, insulated gate bipolar transistors, static induction transistors, static induction thyristors and the like in addition to the GTO as switching elements.

Although embodiments of the present invention, have been described above, the invention is not limited by any of the details of description and that various changes and modifications may be made in the invention without departing from the spirit and scope thereof.

With the present invention, high- and constant-voltage diodes demonstrating stable constant-voltage characteristics are obtainable according to the present invention and when applied to diodes in snubber circuits of semiconductor switching elements and those in power converters such as invertors, circuit elements are prevented from breaking down because of overvoltage resulting from the switching of semiconductor switching elements. Reliable snubber circuits and power converters are thus attained.

What is claimed is:

1. A constant-voltage diode, comprising:

a first semiconductor region of first conductivity type;

a second semiconductor region of a second conductivity type, said second conductivity type being different from said first conductivity type, said first and second semiconductor regions contacting each other such as to form a first pn junction therebetween;

a third semiconductor region of said second conductivity type contacting said second semiconductor region;

a fourth semiconductor region of said first conductivity type contacting and being at least partially surrounded by said second semiconductor region; and

first and second electrodes in electrical contact with said first and third semiconductor regions, respectively;

wherein said third semiconductor region is interposed between said fourth semiconductor region and said second electrode to embed said fourth semiconductor region and separate it from the second electrode;

wherein the impurity concentration of at least one of said first and second semiconductor regions is less than the impurity concentration of at least one of said third and fourth semiconductor regions.

2. A diode according to claim **1**, wherein the impurity concentration of said second semiconductor region is less than the impurity concentration of both said third and fourth semiconductor regions.

3. A diode according to claim **1**, wherein the impurity concentration of said first semiconductor region is less than the impurity concentration of both said third and fourth semiconductor regions.

4. A diode according to claim **1**, wherein said fourth semiconductor region contacts said third semiconductor region such as to form a second pn junction therebetween.

5. A diode according to claim **1**, wherein said fourth semiconductor region is wholly surrounded by said second semiconductor region.

6. A diode according to claim **1**, having an additional semiconductor region of said first conductivity type between said first semiconductor region and said first electrode.

7. A constant-voltage diode, comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type, said second conductivity type being different from said first conductivity type, said first and second semiconductor regions contacting each other such as to form a first pn junction therebetween;

a third semiconductor region of said second conductivity type contacting said second semiconductor region;

a plurality of fourth semiconductor regions of said first conductivity type, each of said plurality of fourth semiconductor regions being at least partially surrounded by said second semiconductor region;

first and second electrodes in electrical contact with said first and third semiconductor regions, respectively;